CTTC
Centre Tecnològic de Telecomunicacions de Catalunya

Technical clauses

Object: Supply of the baseband signal-processing hardware components and software

I. Introduction

The purpose of this document is to define the technical specifications of an experimental testbed that will host a complete baseband signal-processing hardware solution. Special care has been taken to include sufficient processing elements (Field Programmable Gate Arrays - FPGAs, Digital Signal Processors – DSPs) and a number of (inter-)communication interfacing options in the required hardware specifications.

II. General technical specifications

In the following sections it is quoted a detailed and concise description of the required specification of each hardware module; the different signal-processing stages are described as separate boards. Nevertheless, the specified hardware processing solution could also be implemented in a single-board computer or any other combination of boards. The different clauses are divided in the following four categories

1. Technical specifications
2. Training / demonstration
3. Warranty and shipping
4. General clauses and delivery

1. Technical specifications

1a. Analogue to Digital Conversion (ADC) board

- At least six single, 14-bit ADC input channels (e.g. similar to the Analog Devices AD6645) having a guaranteed sample rate of 105 MSPS. Possibility to expand the number of ADC input channels to 16.
- Analogue input bandwidth ranging from 0.2 MHz to (at least) 200 MHz (-3dB), AC-coupled or DC-coupled inputs, with gain.
- -18 dBm to +4 dBm full-scale input.
- On-board clock (i.e. up to 100 MHz) or use of external clock.
- At least one FPGA device similar to the Xilinx Virtex-4 XC4VLX160 (i.e. user custom code integration).
- Sufficiently large (e.g. at least 64-megabit) onboard flash memory to store the FPGA bitstream.

- Each channel should be connected to a programmable gain amplifier before each ADC.
- At least 128-MB SDRAM for data buffering of FPGA data.
- 32-bit wide parallel communication link capable of delivering data rates of at least 400 MBps.
- 32-bit wide general purpose I/O communication interface.
- High-bandwidth data transfers (at least 1 GBps) between two FPGA components (i.e. transmitter and receiver components and interfaces), from which one resides in the ADC board and another one which is located in an external board.
- 32-bit PCI external port with at least 33MHz bus speed configuration.
- Any other I/O options and communication interfaces will be a desirable board-feature.
- Language-based (C and VHDL) board software development (i.e. reference designs, application examples).
- Windows-based graphical user interface for parameter control.
- Model-based design flow for rapid prototyping (i.e. Simulink, Xilinx System Generator).
- Backplane cPCI interface.
- Expansion modules for interconnecting the ADC board with additional processing boards may also be included.

1b. Digital to Analogue Conversion (DAC) board

- At least three dual channel Digital to Analogue Converters (e.g. similar to the Texas Instruments DAC5687) having a maximum sampling rate of 480 MSPS (14-bit resolution), with 3x interpolation and incoming data sample rate of 120 MSPS (14-bit sample). Future upgrade to 16 channels should be an option.
- 0.3-MHz to (at least) 240-MHz analog output bandwidth (–3 dB), AC coupled, with gain.
- –21-dBm to 2.9-dBm full-scale output (e.g. programmable gain).
- On-board clock (i.e. at least 100 MHz) or use of external clock.
- At least one FPGA device similar to the Xilinx Virtex-4 XC4VLX160 (i.e. user custom code integration).
- Sufficiently large (e.g. at least 64-megabit) onboard flash memory to store the FPGA bitstream.
- At least 128-MB SDRAM for data buffering of FPGA data.
- 32-bit wide parallel communication link capable of delivering data rates of at least 400 MBps.
- 32-bit wide general purpose I/O communication interface.
- High-bandwidth data transfers (at least 1 GBps) between two FPGA devices (i.e. transmitter/receiver components and interfaces), from which one resides in the DAC board and another one which is located in an external board.
- 32-bit PCI external port with at least 33MHz bus speed configuration.
- Any other I/O options and communication interfaces will be a desirable board-feature.
- Language-based (C and VHDL) board software development (i.e. reference designs, application examples.
- Windows-based graphical user interface for parameter control.
- Model-based design flow for rapid prototyping.

- Backplane cPCI interface.
- Expansion modules for interconnecting the DAC board with additional processing boards may also be included.
- Documentation and software CDs/DVDs, or download access to a secure site (i.e. through ssh, sftp) must be included.

1c. Baseboard and chassis

- At least 2 FPGA devices similar to the Xilinx Virtex-4 XC4VLX160 for system prototyping.
- At least 4 DSPs, 8000 MIPS at 1000 MHz (e.g. similar to the Texas Instruments TMS320C6416).
- At least 128 MB external SDRAM per DSP and per FPGA.
- High-bandwidth data transfers (at least 1 GBps) between two FPGA devices (i.e. transmitter and receiver components and interfaces), from which one resides in the baseboard and another one which is located in an external board.
- High-bandwidth data transfers (at least 1 GBps) between the on-board FPGA devices (i.e. transmitter and receiver components and interfaces).
- JTAG connector to all DSP for debugging.
- JTAG connector to all FPGA for debugging.
- Onboard GPIO troubleshooting port.
- Any other I/O options and communication interfaces will be a desirable board-feature.
- Language-based (C and VHDL) board software development (i.e. reference designs, application examples). Reference designs on how to interface with the ADC/DAC stages must also be provided.
- Windows-based graphical user interface for parameter control.
- Model-based design flow for rapid prototyping.
- Backplane cPCI interface.
- Expansion connectors for mounting additional boards to the baseboard may also be included.
- cPCI chassis system (1x3U or 1x6U form factor) with at least 6 cPCI slots, cPCI CPU (i.e. 2GHz) for control purposes, 1 GB additional SDRAM.
- Documentation and software CDs/DVDs, or download access to a secure site (i.e. through ssh, sftp) must be included.

2. Training / demonstration

- As part of the offer the third party agrees to provide technical training (2 days) and set up a demonstration of the boards without introducing additional charges to the final offer.
- The agenda of the training/demonstration has to focus on the particular design requirements set by the CTTC; the details of this agenda will be mutually agreed in advance.

3. Warranty and shipping

- A minimum of one year warranty which will cover hardware, software updates and technical support.

- If a board needs replacement and/or repairing during the warranty period the third party agrees to cover the cost of shipping and insurance.
- The shipping of the products should include insurance.

4. General clauses and delivery

- The system must include all the necessary cables, connectors, accessories, power supply units, AC/DC converters, adaptors and any other required parts that will make the system fully functional upon delivery.
- The third party must have qualified engineers able to provide technical support and maintenance should this be required during the warranty period.
- The products should be in working condition upon delivery.
- Maximum delivery lead-time of 8 weeks.
- The shipping of the products should include insurance.